REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-71 were pending and rejected. In this response, no claim has been canceled. Claims 1, 24, 40, and 56 have been amended. No new matter has been added.

The Examiner has rejected claims 1-4, 10, 12-13, 19-29, 33, 37-45, 49, 53-61, 65 and 70-71 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,822,606 to Morton ("Morton"), in view of U.S. Patent No. 5,497,465 to Chin, et al. ("Chin"). Claims 5-9, 11, 30-32, 46-48 and 62-64 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Morton in view of Chin as applied to claims 1-4, 24, 40 and 56 above, and further in view of U.S. Patent No. 5,430,884 to Beard, et al. ("Beard"). Claims 14-18, 34-36, 50-52 and 66-68 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Morton in view of Chin as applied to claims 1, 24, 40 and 56, and further in view of U.S. Patent No. 6,597,745 to Dowling ("Dowling"). In view of the foregoing amendments, it is respectfully submitted that 1-71 as amended include limitations that are not disclosed or suggested by the cited references, individually or in combination.

Specifically, for example, independent claim 1 recites as follows:

> 1. An apparatus, in an integrated circuit (IC) of a data processing system having at least one host processor and host memory, comprising:
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> a chip interconnect;
>
> a host interface coupled to the chip interconnect for interfacing the IC with the at least one host processor external to the IC;
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> a memory interface coupled to the chip interconnect for interfacing the IC with the host memory external to the IC;
>
> a memory controller coupled to the chip interconnect for controlling the host memory comprising DRAM memory via the memory interface;
>
> a scalar processing unit coupled to the chip interconnect, the scalar processing unit being capable of executing instructions to perform scalar data processing;

a vector processing unit coupled to the chip interconnect, the vector processing unit being capable of executing instructions to perform vector data processing; and

an input and output (I/O) interface coupled to the chip interconnect for interfacing the IC with an I/O controller of the data processing system, the I/O controller being external to the IC for controlling I/O devices of the data processing system, wherein the chip interconnect, the memory controller, the scalar processing unit, the vector processing unit, the I/O interface, the host interface, and the memory interface are implemented within the IC which is a single chipset interfacing the at least one host processor and the host memory with other components of the data processing system, including the I/O controller and the I/O devices.

(Emphasis added)

Independent claim 1 requires a scalar processing unit and a vector processing unit implemented within a single chipset that interfaces one or more host processors and host memory with other components of a data processing system, such as I/O controller and the I/O devices of the data processing system, where the host processor and the host memory are external to the chipset. It is respectfully submitted that a chipset having memory controller to interface with a host processor (e.g., CPU) and the host memory with other components of a computer (e.g., I/O controller and I/O devices) is also be referred to as a "north bridge" in the computer art, while the I/O controller is also referred to as a "south bridge" in the art since it is "south" of the north bridge in view of the processor and host memory. It is respectfully submitted that these limitations are absent from the cited references.

Rather, Morton is related to a DSP (digital signal processing) chip (see Abstract of Morton) that is a special processor that is running in parallel and is normally plugged into an I/O bus of a computer system outside of the chipset (e.g., a north bridge), and typically communicate with the host processor via the I/O controller.

In fact, Morton distinguishes the DSP chip as part of Morton's invention from an ordinary microprocessor such as a family of x86 chips (e.g., host processor). See, for example, col. 2, line 18 to col. 3, line 37 of Morton.

Specifically, Morton states:

> "The invention is primarily intended to assist in the handling and processing of large amounts of numeric data in real time at low cost, while consuming a minimum of power and occupying a minimum of space. Such applications generally fall under the catergory of real time digital signal processing."

(Morton, col. 2, lines 7-16, emphasis added)

Thus, the DSP chip of Morton is not implemented in a single chipset (e.g., a north bridge having a memory controller) that interfaces a host processor and host memory with the rest of components of a computer (e.g., single computer). Rather, the DSP chip of Morton is an additional plug-in component that "assists" in handling and processing large amounts of numeric data.

Although the Office Action acknowledged that Morton did not specifically teach a single chipset; nevertheless, the Office Action contended that Chin (e.g., Fig. 1, host 24) teaches a single chip set (4/3/2006 Office Action, page 4). Applicant respectfully disagrees.

Similar to Morton, Chin is related to parallel digital processing system such as MIMD using optical interconnection between control sections and data processing sections (see Abstract of Chin).

Specifically, referring to Fig. 1 of Chin, the host 24 is optically coupled to processing system 10. Both host 24 and system 10 are separate systems. For example, Chin states:

> "FIG. 1 illustrates the overall configuration of a computer system according to this invention. The area enclosed by dotted lines in the figure is a computer system 10 using optical input. The computer system 10 comprises a control section 12 consisting of n memory elements 1-1, 1-2, . . . , 1-n each having an instruction memory and a data memory, and n controllers 2-1, 2-2, . . . , 2-n; a driver section 14 consisting of n LED

drivers 3-1, 3-2, . . . , 3-n; an LED array section 16 consisting of n LED arrays 4-1, 4-2, . . . , 4-n; a processing section 20 consisting of n processors 5-1, 5-2, . . . , 5-n each having an optical input section that is capable of photoelectric conversion; an optical interconnection section 18 optically interconnecting the LED array section 16 and the processing section 20; a system control section 22 controlling the controllers of the control section 12.

...

The program decoded and compiled by the host computer 24 is stored in n instruction memory elements via n controllers. Data are also stored in n data memories. The data memories are flexibly constructed using only high-speed memories or using both high-speed and low-speed memories as necessary. Although controllers read data from their respective high-speed memories, when high-speed and low-speed memories are used in combination, data transfer to and from both types of memories is accomplished by the DMA (direct memory access) section of the controller.

...

Processors are arranged into arrays on processor chips, which are fewer in number than LED array chips. Each processor receives control and data signals needed to execute operations, which are subject to photoelectric conversion in parallel in an optical input section. The digital signals converted into electrical signals are latched and amplified, and execute operations in synchronism with the clock of the processor. Since a large number of processors are mounted on a single processor chip, a large quantity of control and data signals are used to implement parallel processing. It is difficult to provide such a large quantity of electrical input connectors on a chip. Connections by propagating optical signals according to this invention successfully-solves this difficulty."

(Chin, col. 5, line 66 to col. 67, line 12, emphasis added)

Thus, Chin teaches multiple special processors (e.g., together as system 10) plugged in a host computer 24, which is typically a well-known MIMD system. Such a design is not the same as an integrated a north bridge having a memory controller with a vector and scalar processing units as required in independent claim 1 of the present application.

In addition, there is no suggestion within Morton and Chin to combine with each other. The designs and approaches of Morton and Chin are significantly different. It is respectfully submitted that one with ordinary skill in the art would not, based on the teachings

of Morton and Chin, to combine these two references because such a combination lacks reasonable expectation of success. Even if they were combined, such a combination still lacks the limitations set forth above.

It is respectfully submitted that Beard and Dowling also fails to disclose the limitations set forth above. Therefore, for the reasons set forth above, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claims 24, 40, and 56 include limitations similar to those discussed above. Thus, for the reasons similar to those discussed above, it is respectfully submitted that claims 24, 40, and 56 are patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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